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Recent Advances in Low-Cost Multi-GigaHertz Testing

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Abstract

This presentation provides a summary and status of three on-going research projects that are developing new low-cost techniques for testing devices with multiple channels of high-speed (>1 GHz) data. Each project uses commercially-available components to keep costs low, and provides the circuits necessary for testing specific applications. This presentation provides a summary of these projects, recent achievements, and future directions. Further details will soon be available in two papers at the 2003 International Test Conference [1,2].

In the first project [1], we enhance existing automated test systems by adding multiplexing logic and high-speed sampling circuits. Modular circuits are added to the loadboard, and interface to both the "host" ATE and the device under test. Each module supports 12 high-speed differential signals with data rates as high as 2.5 Gbps. The present system is expandable up to 12 modules, so that as many as 144 differential pairs can be tested. The present system has stable performance up to 2.5 Gbps, with typical timing accuracy of ±25ps and OTA under 100ps. Current efforts are focused at extending to 3.2Gbps and above.

In the second project [2], an FPGA-based digital logic core (DLC) is used to provide a stand-alone programmable tester. The DLC produces moderate-speed (100-300 Mbps) data signals which are formatted and/or multiplexed using PECL devices to create sub-picosecond bit periods, and multi-gigabit-per-second signals. These interface to optoelectronic components which modulate lasers of different wavelengths. The optical signals are combined at the transmitting end, and optically split at the receiving end (to recover the parallel data words). The present system is designed as a "test bed" for the evaluation of various OE and EO techniques. We have 5 channels for both transmitting and receiving, to support a 4-bit parallel data word and a "data valid" signaling bit. The end-application will require extending this to words with at least 64 bits, and perhaps as many as 256 bits. Minimum bit widths have been demonstrated at 300ps, with timing resolution of 10ps, and comparable timing accuracy. The objective is to provide low-latency transfer of small data packets within clusters of supercomputers.

In the third project [2], a similar DLC is combined with multiplexing and sampling PECL circuits to create a self-contained tester for checking high-speed data paths in a wafer-probing environment. The "mini-tester" is designed to fit on the top side of a probe card, requiring only a source of power, a single RF clock signal, and a USB connection to a personal computer. The mini-tester produces a programmable data source up to 4.4 Gbps with 10ps timing resolution. A high-speed PECL sampling circuit is designed to capture the returned signal, also with 10ps resolution.

References:

[1] D.C. Keezer, D. Minier, M.C. Caron, "A Production-Oriented Multiplexing System for Testing above 2.5 Gbps," to be presented at the Intl. Test Conf., Sept./Oct. 2003.

[2] J.S.Davis, D.C. Keezer, K. Bergman, O. Liboiron-Labouceur, "Application and Demonstration of a Digital Test Core: Optoelectronic Test Bed and Wafer-level Prober," to be presented at the Intl. Test Conf., Sept./Oct. 2003.