Low-Cost Strategies for Testing Multi-GigaHertz SOPs and Components

D.C. Keezer[1], J. S. Davis[2], S. Bezos[1], D. Minier[3], M.C. Caron[3],
K. Bergman[4], O. Liboiron-Labouceur[4]
1- Georgia Institute of Technology, Atlanta, GA
2- Mississippi State University, MS
3- IBM, Canada, Bromont, Canada
4- Columbia University, New York, NY

Abstract

This presentation provides a summary and status of three on-going research projects that are developing new low-cost techniques for testing devices with multiple signals of high-speed (>1 GHz) data. Each project uses commercially available components to keep costs low, and provides the circuits necessary for testing specific applications. This presentation provides a summary of these projects, recent achievements, and future directions as they might apply to testing system-on-package (SOP) and other components. Further details are available in two papers recently presented at the 2003 International Test Conference [1,2].

1. Introduction

Without exception, all technology roadmaps indicate a relentless increase in clock and data rates for advanced components into the forseeable future. Certainly the performance of future test equipment will continue to increase as well. However, these improvements tend to be incremental. They also tend to lag the performance of leading edge components, since the test equipment itself is made up of electronics components. Therefore, there is a need for new test methods that do not rely upon rapid test equipment advances.

To this end, we have introduced the concept of the "test support processor" (TSP) [3], and more recently have extended this to include self-contained "miniature testers" [2]. A TSP is a customized circuit which is added to an existing automated test system in order to enhance either the performance or to provide additional test functionality. Because the TSP is customized for specific applications, it can take advantage of newly-developed components that surpass existing test system performance.

By extending the TSP to operate without the aid of automated test equipment, a self-contained miniature tester can be constructed. The customized miniature tester will not likely have the wide range of features available in automated test equipment (ATE). However it is designed to provide only the specific test features needed for a particular application.

In the first project [1], we enhance existing automated test systems by adding multiplexing logic and high-speed sampling circuits. Modular circuits are added to the load-board, and interface to both the "host" ATE and the device under test. Each module supports 12 high-speed differential signals with data rates as high as 2.5 Gbps. The present system is expandable up to 12 modules, so that as many as 144 differential pairs can be tested. The present system has stable performance up to 2.5 Gbps, with typical timing accuracy of $\pm$25ps and OTA under 100ps. Current efforts are focused at extending to 3.2Gbps and above.

In the second project [2], an FPGA-based digital test core (DTC) [4] is used to provide a stand-alone programmable tester. The DTC produces moderate-speed (100-300 Mbps) data signals that are formatted and/or multiplexed using PECL devices to create sub-picosecond bit periods, and multi-gigabit-per-second signals. These interface to optoelectronic components that modulate lasers of different wavelengths. The optical signals are combined at the transmitting end, and optically split at the receiving end (to recover the parallel data words). The present system is designed as a "test bed" for the evaluation of various OE and EO techniques. We have 5 channels for both transmitting and receiving, to support a 4-bit parallel data word and a "data valid" signaling bit. The end-application will require extending this to words with at least 64 bits, and perhaps as many as 256 bits. Minimum bit widths have been demonstrated at 300ps, with timing resolution of 10ps, and comparable timing accuracy. The objective is to provide low-latency transfer of small data packets within clusters of supercomputers.

In the third project [2], a similar DTC is combined with multiplexing and sampling PECL circuits to create a self-contained tester for checking high-speed data paths in a wafer-probing environment. The "mini-tester" is designed to fit on the top side of a probe card, requiring only a source of power, a single RF clock signal, and a USB connection to a personal computer. The mini-tester produces a programmable data source up to 4.4 Gbps with 10ps timing resolution. A high-speed PECL sampling circuit is designed to capture the returned signal, also with 10ps resolution

2. Test-Support Multiplexers and Demultiplexers

One of the most difficult challenges encountered in testing today results from the need to support high data rates while maintaining appropriately tight timing accuracy. Since typical automated test systems are limited to 1 or 2 Gbps, and since devices often require higher speeds, we must find ways to test these higher-speed components and subsytems using existing test

equipment. One way to do this is to logically combine several test signals in order to form a single channel with a higher data rate. This multiplexing scheme can be replicated to produce many high-speed signals if needed. A complemetary technique (demultiplexing or sampling) can be used to capture the circuit-unter-test output responses.

An example test configuration is shown in **Fig.1** where "Driver" multiplexing modules and "Receiver" demultiplexing modules are added to the traditional ATE environment. Here the combination of the Driver and Reciever modules with a customized loadboard creates an "active loadboard" arrangement.

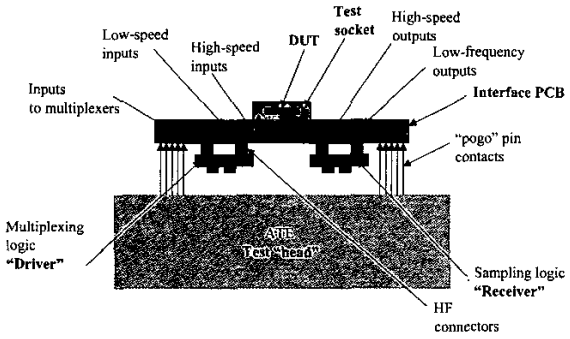

Figure 1. Driver (multiplexers) and Receiver (sampling) modules added to an ATE test interface loadboard [1].

To demonstrate the use of such Driver and Receiver modules, a specific application is illustrated in **Fig.2**. Here two 8-channel 4:1 multiplexer modules, and two 8-channel 1:4 demultiplexer modules are used to test 16 high-speed differential channels of an AMCC S2018 17x17 crosspoint switch. The device operates at 3.2 Gbps on each channel. For this demonstration the host ATE is an Agilent 93000-P1000 with almost 900 channels, each capable of speeds up to 1 Gbps.

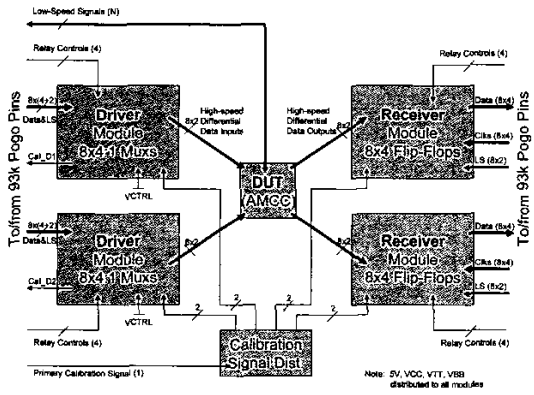

Figure 2. High speed test application for a 3.2Gbps 17x17 crosspoint switch [1].

Figure 3 shows a photograph of the bottom side of the active loadboard, with one each of the Driver and Receiver modules mounted.

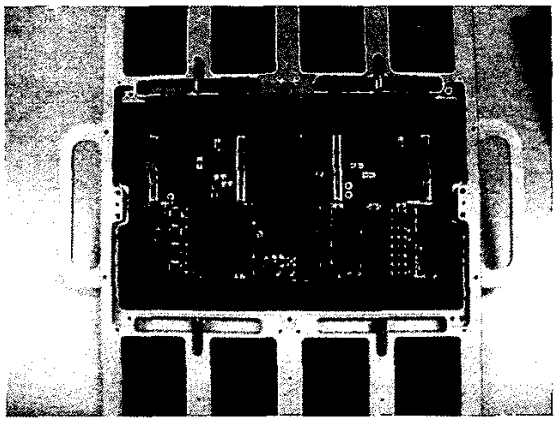

Figure 3. Bottom view of the active test interface loadboard, showing one each of the Driver and Receiver Modules [1].

Positive emitter-coupled logic (PECL) is used to implement the Driver and Receiver modules. A variety of multigigahertz PECL devices are readily available for such applications. The particular parts used in this demonstration exhibit transition times on the order of 150ps. An example "eye" diagram is illustrated in **Fig.4**. This shows one of the Driver channel outputs at 1Gbps. Notice the fast and symmetric rise and fall times as well as the modest amount of jitter which results in an open "eye" pattern. This signal was measured from an air-cooled prototype Driver module. In an improved, water-cooled version used better relays to obtain good performance at 2.5 Gbps as illustrated in **Fig.5**.

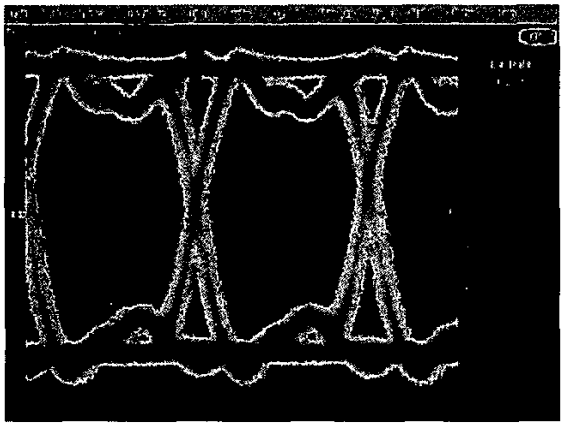

Figure 4. Driver module output eye diagram at 1 Gbps.

Figure 5. Water-cooled production driver module output at 2.5 Gbps [1].

Producing well-controlled multi-gigahertz input signals is only half of the problem. A complete solution also requires that the output signals be captured and compared to expected responses. The Receiver modules are constructed using advanced PECL in order to implement the 1-to-4 demultiplexing function for each multi-gigahertz output channel. The specific demultiplexing circuit implemented allowed the sampling clock timing to be controlled from the host ATE. This permits characterization testing to find the precise timing value for any output logic transition. If the sampling clock is swept across several edges, while the ATE records the measured logic state, then the logic timing diagram can be obtained as illustrated in **Fig.6**. Here a 2 Gbps test signal is effectively digitized in 40ps increments. The limit of resolution for this demonstration was actually a factor of four better (10ps).

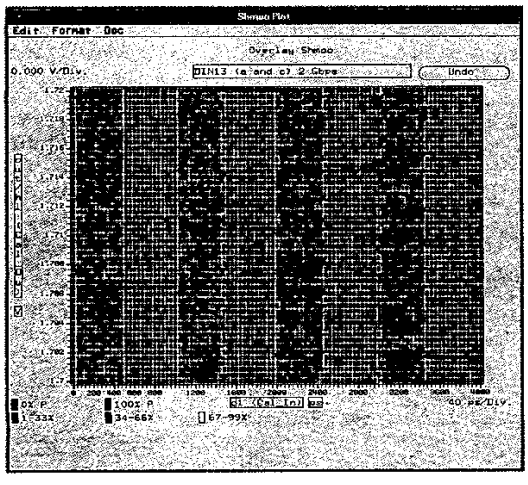

Figure 6. Receiver module sampling at 2 Gbps [1].

3. Optical Test Bed Application

In order to provide for more complex logic functions in the Test Support Processor (TSP), we have developed a general-purpose, reusable programmable logic design called the Digital Test Core (DTC). The basic components of this design are illustrated in **Fig.7**. The central component is a 300k gate FPGA (Xilinx XCV300E). In addition, the DTC includes a specialized microcontroller chip for interfacing to a Universal Serial Bus (USB). Supporting these are a 12 MHz crystal oscillator, and an EEPROM (or FLASH memory). The crystal provides a clock for the USB standard, and the PROM stores the personalization data for the FPGA (which is downloaded upon power-up). A high-speed port to optional SRAM is also part of the design. About 90 signals are available as general-purpose I/O to support specific test applications.

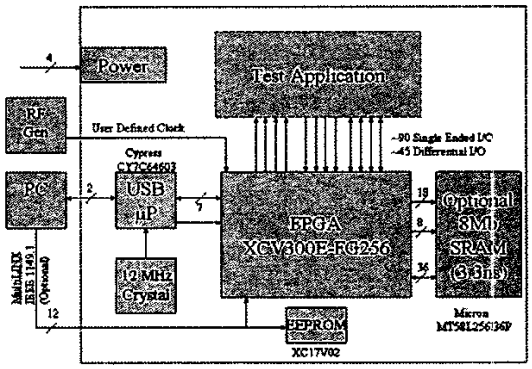

Figure 7. Digital Test Core used for several test applications [2].

For the second project, we needed to create very precisely-timed logic signals to emulate the behavior of a parallel slice from a microprocessor-to-memory communication channel. These signals were eventually used to control laser drivers which effectively converted the signals to light pulses of differing wavelengths. An example of the desired wave shapes is shown in **Fig.8**. Here four example data bits are synchronously produced to emulate the behavior of part of a much wider data buss. A "presence" bit is also produced to signal when the data is valid.

The relative timing for leading and trailing edges for both data and presence signals must be controlled with 10ps accuracy in the Optical Test Bed. A 10ns range for the placement of these edges is also required. The design of the PECL circuits to produce these signals paid careful attention to maintaining timing accuracy and to minimization of jitter. **Figure 9** shows an early version of the Optical Test Bed electronics. This includes the DTC as well as PECL circuits for the transmitting and receiving functions. The SMA connectors on the right side of the board are for connection to/from the optical components.

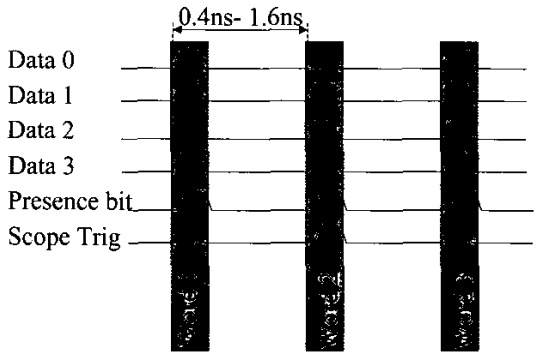

Figure 8. Test stimuli signals needed for the Optical Test Bed application [2].

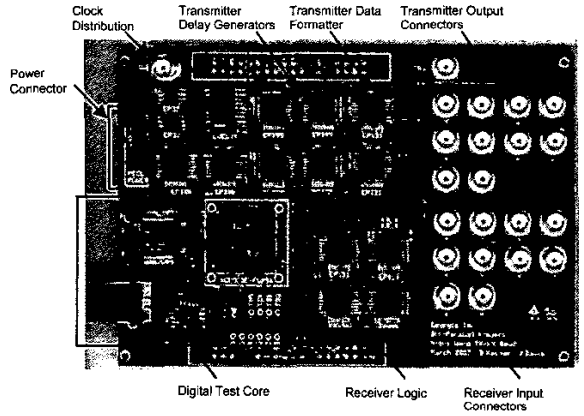

Figure 9. Transmitter and Receiver electronics used for the Optical Test Bed application [2].

Some example waveforms are illustrated in **Fig.10**. These are similar to the desired patterns illustrated in Fig.8. Here the four data signals are shown for two consecutive parallel words.

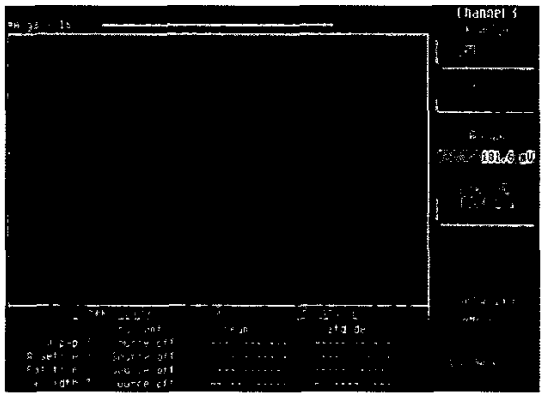

Figure 10. Example measured transmitter data signals for the Optical Test Bed application [2].

4. Miniature Tester for parallel Wafer-Level Probing

For testing Wafer Level Packaged (WLP) devices, the availability of miniature compliant leads may be exploited for testing at the wafer level. These leads, which are primarily intended to serve as the next level of interconnect when the dies are eventually mounted, are lithographically patterned on to the wafer surface and provide a potential way to electrically contact the chips. However, the extremely high density that is possible with WLP means that careful attention must be focused at this interface. With this in mind, an interposer is illustrated in **Fig.11** to redistribute the high density WLP signals to a macroscopic scale (similar to a micro-BGA). A customized "Mini-Tester" based on the Digital Test Core is illustrated as a self-contained module mounted to the top side of a multi-layer printed circuit board which serves in place of the traditional probe card. Connections to the miniature tester are limited to: power, USB, and a high-performance (low-jitter, multi-gigahertz) clock input.

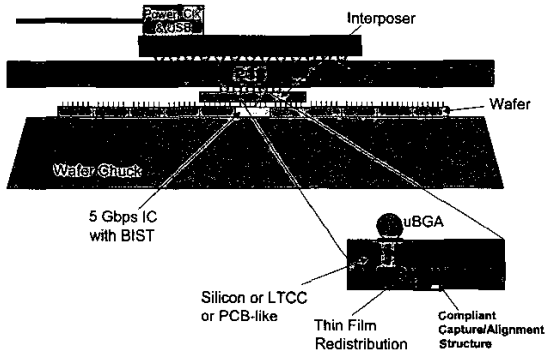

Figure 11. High-speed wafer-probe testing of wafer-level packaged (WLP) devices using a "miniature tester" and a high-density interposer [2].

Since the WLP compliant leads are available on all the die sites, the miniature tester could be replicated and arranged into an array as illustrated in **Fig.12**. This would permit parallel, at-speed functional testing and result in a production throughput increase of about an order of magnitude. Notice that only a small number of signals are required for each mini-tester, so the complexity of the PCB can be minimized. Such aggressive use of WLP for testing has not yet been demonstrated. However, this strategy is a logical extension of existing parallel tests (such as used in memory testing) and as an extension of the TSP/mini-tester approach.

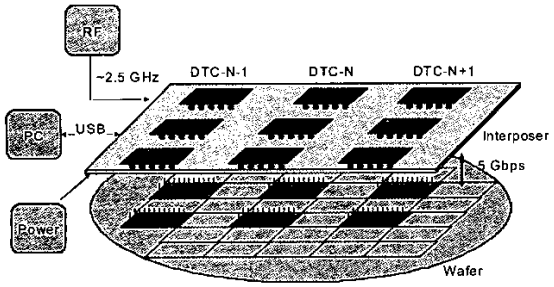

Figure 12. Parallel high-speed wafer probing using multiple miniature testers [2].

An example board-level prototype for such a miniature tester is shown in **Fig.13**. This solution again uses the Digital Test Core to provide general-purpose communication to a PC through the USB, and to implement the state-machine logic for controlling some specific tests. The tests are designed to demonstrate high-speed (~5Gbps) signal propagation through the compliant lead structures. Therefore both stimulus generation and signal sampling is required at this high rate. To accomplished this, PECL circuits are added to the DTC which implement signal-multiplexing and picosecond sampling.

Since the FPGA in the DTC is limited to about 311 Mbps per signal, two groups of eight such signals are multiplexed to form two independent data sources at 2.5 Gbps. These are then combined in a second-stage multiplexer to obtain the higher speed signal. Some example waveforms are illustrated in **Fig.14** (at slightly lower speeds).

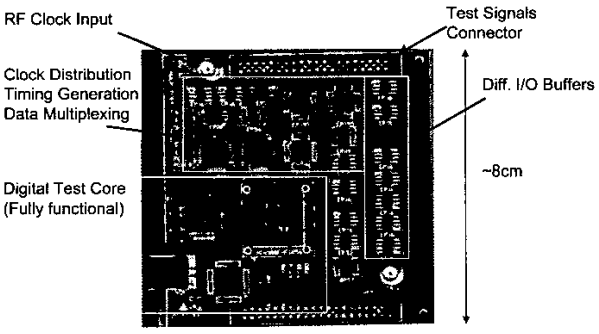

Figure 13. Prototype miniature tester with embedded Digital Test Core [2].

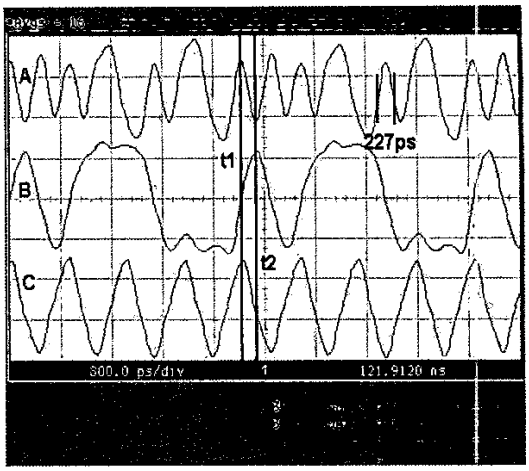

Figure 14. Example test signals from the prototype miniature tester at (a) 4.4 Gbps, and (b,c) 2.2 Gbps [2].

5. Conclusions

In this paper we have described three examples of how customized circuits can be incorporated into the production testing environment to achieve improved test performance (multi-gigahertz signal speeds), specialized test functions, and/or reduced test cost. Lower cost may result from the use of autonomous testers that permit economical parallel testing.

Acknowledgments

This work was supported in part by the National Science Foundation under contract EEC-9402723. The National Science Foundation supports the Georgia Tech Packaging Research Center (PRC) as a NSF Engineering Research Center.

References

1. D.C. Keezer, D. Minier, M.C. Caron, "A Production-Oriented Multiplexing System for Testing above 2.5 Gbps," *Proc. of the Intl. Test Conf.*, Sept./Oct. 2003.
2. J.S.Davis, D.C. Keezer, K. Bergman, O. Liboiron-Labouceur, "Application and Demonstration of a Digital Test Core: Optoelectronic Test Bed and Wafer-level Prober," *Proc. of the Intl. Test Conf.*, Sept./Oct. 2003.
3. D. C. Keezer, Q. Zhou, "Test Support Processors for Enhanced Testability of High-Performance Circuits," *Proc. of the Intl. Test Conf.*, Baltimore, MD, October 1999, pp. 801-809.
4. J.S. Davis, D.C. Keezer, "Multi-Purpose Digital Test Core Utilizing Programmable Logic," *Proc. of the Intl. Test Conf.*, Baltimore, MD, October 2002, pp. 438-445.